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Document Listing

Document	Image pages	Text pages	Error pages
US 5825057 A	0	18	0
Total	0	18	0

DOCUMENT-IDENTIFIER: US 5825057 A
TITLE: Process for fabricating layered superlattice materials and making
electronic devices including same

APD:
19941205

BSPR:
The invention in general relates to the fabrication of layered superlattice
materials, and more particularly to fabrication processes that provide low
fatigue **ferroelectric** and reliable high dielectric constant integrated circuit
devices that are unusually resistant to degradation.

BSPR:
Copending U.S. patent application Ser. No. 07/965,190 filed Oct. 23, 1992
discloses that the layered superlattice materials discovered by G. A.
Smolenskii, V. A. Isupov, and A. I. Agranovskaya (See Chapter 15 of the book,
Ferroelectrics and Related Materials, ISSN 0275-9608, [V.3 of the series
Ferroelectrics and Related Phenomena, 1984] edited by G. A. Smolenskii,
especially sections 15.3-15) are far better suited for **ferroelectric** and high
dielectric constant integrated circuit applications than any prior materials
used for these applications. These layered superlattice materials comprise
complex oxides of metals, such as strontium, calcium, barium, bismuth, cadmium,
lead, titanium, tantalum, hafnium, tungsten, niobium zirconium, bismuth,
scandium, yttrium, lanthanum, antimony, chromium, and thallium that
spontaneously form layered superlattices, i.e. crystalline lattices that
include alternating layers of distinctly different sublattices, such as a
ferroelectric and non-**ferroelectric** sublattices. Generally, each layered
superlattice material will include two or more of the above metals; for

example, strontium, bismuth and tantalum form the layered superlattice material strontium bismuth tantalate, SrBi.sub.2 Ta.sub.2 O.sub.9. Copending U.S. patent application Ser. No. 07/981,133, describes a method of fabricating layered superlattice thin films that results in electronic properties for these materials several times better than the best previously known. This disclosure more fully develops certain aspects of the previous application, and discloses improvements in the fabrication process that together approximately double the values of the critical **ferroelectric** parameters, such as the polarizability, over the values obtained with the basic process described in the copending 981,133 application.

BSPR:
In addition to having good values of the **ferroelectric** parameters, it is also important that the physical quality of the **ferroelectric** films be suitable for use in manufacturing processes. For example, the film should have a relatively uniform grain size, which results in better crystalline quality, i.e films free of cracks and other defects. The film grain size should also be small compared to the thickness of the film; otherwise the roughness of the film can be comparable to the thickness and other dimensions of the device components, which makes it difficult or impossible to fabricate devices within tolerances and results in short circuits and other electrical breakdowns. Further, it is important that the fabrication processes be ones that can be performed relatively rapidly, since long processes are more expensive in terms of the use of facilities and personnel.

BSPR:
Rapid thermal processing and furnace annealing in an atmosphere of oxygen are several of many processes that are well-known in the thin-film fabrication

technology, See for example, "Process Optimization and Characterization of
Device Worthy Sol-Gel Based PZT for **Ferroelectric** Memories", B. M. Melnick, J.
D. Cuchiaro, L. D. McMillan, C. A. Paz De Araujo, and J. F. Scott in
Ferroelectrics, Vol 109, pp. 1-23 (1990). It is also known to add excess lead
in fabricating PZT using a spin-on and annealing process to account for lead
lost as lead oxide vapor in the fabrication process. See U.S. Pat. No.
5,028,455 issued to William D. Miller et al. It is also known to add excess
Bi.sub.2 O.sub.3 when fabricating a bismuth titanate thin film using sputtering
to compensate for the loss of this component in the sputtering process. See "A
New **Ferroelectric** Memory Device,
Metal-**Ferroelectric-Semiconductor** Transistor",
by Shu-Yau Wu, IEEE Transactions On Electron Devices, August 1974, pp.
499-504. E. C. Subbarao, in "A Family of **Ferroelectric** Bismuth Compounds", J.
Phys. Chem. Solids, V. 23, pp. 665-676; (1962), discloses the creation of
solid solutions of some layered superlattice materials and that several of
their physical parameters, i.e., the dielectric constant and Curie temperature
change as the proportions of the various elements comprising the solid solution
change. However, these are only some of the hundreds of processes and
parameters that potentially can affect the quality of a layered superlattice
material, and prior to the work of the present inventors, how to use these and
other fabrication parameters to arrive at **ferroelectric** properties such as
extremely low fatigue rates and polarizabilities as high as 25 in layered
superlattice materials was unknown, despite the fact that those skilled in the
art had been searching for materials with such properties for more than thirty
years.

BSPR:
When the layered superlattice material comprises a thin

ferroelectric film which forms the material between the two electrodes of a capacitor, the best results are obtained if a first furnace anneal is performed after the layered superlattice material is formed and a second furnace anneal is performed after the second **electrode** is deposited. The second anneal may take place before or after the capacitor is patterned, or alternatively, a second anneal may be performed prior to patterning and a third anneal performed after patterning. The second and third anneal processes are performed at a temperature lower than the first anneal temperature.

BSPR:
If one of the metals is bismuth, the polarizability of the **ferroelectric** is greatly enhanced if about 125% of the normal stoichiometric amount of bismuth is added.

BSPR:
The above method of designing an electrical or electronic device is particularly applicable to devices including layered superlattice materials that include solid solutions of several layered superlattice compounds. In this aspect the invention solves the problem of fabricating high performance **ferroelectric** and high dielectric constant devices by providing a method of making an electrical or electronic device, the method comprising: providing a record of the values of one or more electronic properties of a layered superlattice solid solution as a substantially continuous function of the proportion of the components of the solid solution; selecting a solid solution from the record with a composition having a desired value of at least one electronic property; and fabricating an electrical or electronic device including a layered superlattice material having the selected composition. The electronic properties may comprise one or more properties

selected from the group comprising polarizability, coercive field, leakage current, dielectric constant, and fatigue. The elements that form the solid solution may include elements selected from the group comprising tantalum, niobium, titanium, zirconium and many other elements.

BSPR:
The methods described above result in layered superlattice materials with excellent electronic properties. For example, **ferroelectric** layered superlattice materials with polarizabilities, 2Pr, higher than 25 microcoulombs per square centimeter have been fabricated. Numerous other features, objects and advantages of the invention will become apparent from the following description when read in conjunction with the accompanying drawings.

DRPR:
FIG. 16 shows graphs of 2Pr versus second **anneal** time for samples of strontium bismuth tantalate prepared with 10% excess bismuth and under atmospheres of **oxygen and nitrogen**;

DEPR:
Directing attention to FIGS. 2 and 3, a wafer 10 containing numerous capacitors 12, 14, 16 etc. is shown. FIG. 2 is a top view of the wafer 10 on which the thin film capacitors 12, 14, 16 etc. fabricated by the process according to the invention are shown greatly enlarged. FIG. 3 is a portion of a cross-section of FIG. 2 taken through the lines 3--3 bisecting capacitor 16. Referring to FIG. 3, the wafer 10 includes a silicon substrate 22, a silicon dioxide insulating layer 24, a thin layer of titanium 26 which assists the next layer, which is a platinum **electrode** 28, in adhering to the silicon dioxide 24, a layer of layered superlattice material 30, and another platinum **electrode** 32. After the layers 24, 26, 28, 30, and 32, are deposited, the wafer

is etched down to layer 28 to form the individual capacitors 12, 14, 16, etc. which are interconnected by the bottom **electrode** 28. The inventionprimarily involves the method of creating the layer 30 of layered superlattice material. As mentioned above, these layered superlattice materials comprise complex oxides of metals, such as strontium, calcium, barium, bismuth, cadmium, lead, titanium, tantalum, hafnium, tungsten, niobium zirconium, bismuth, scandium, yttrium, lanthanum, antimony, chromium, and thallium that spontaneously form layered superlattices, i.e. crystalline lattices that include alternating layers of distinctly different sublattices. Generally each layered superlattice material will include two or more of the above metals; for example, barium, bismuth and niobium form the layered superlattice material barium bismuth niobate, BaBi.sub.2 Nb.sub.2 O.sub.9. The material 30 may be a dielectric, a **ferroelectric,** or both. If it is a dielectric, the capacitor 16 is a dielectric capacitor, and if the material 30 is a **ferroelectric,** then capacitor 16 is a **ferroelectric** capacitor. The layered superlattice materials may be summarized more generally under the formula:

DEPR:
FIG. 4 shows an example of the integration of a layered superlattice capacitor 72 into a DRAM memory cell to form an integrated circuit 70 such as may be fabricated using the invention. The memory cell 50 includes a silicon substrate 51, field oxide areas 54, and two electrically interconnected electrical devices, a transistor 71 and a **ferroelectric** switching capacitor 72. Transistor 71 includes a gate 73, a source 74, and a drain 75. Capacitor 72 includes first **electrode** 58, **ferroelectric** layered superlattice material 60, and second **electrode** 77. Insulators, such as 56, separate the devices 71, 72,

except where drain 75 of transistor 71 is connected to first **electrode** 58 of capacitor 72. Electrical contacts, such as 47 and 78 make electrical connection to the devices 71, 72 to other parts of the integrated circuit 70. A detailed example of the complete fabrication process for an integrated circuit memory cell as shown in FIG. 4 is given in U.S. patent application Ser. No. 919,186, which is incorporated herein by reference. It should be understood that FIGS. 2, 3, 4 depicting the capacitors 12, 14, 16 etc. and integrated circuit 70 are not meant to be actual cross-sectional views of any particular portion of an actual electronic device, but are merely idealized representations which are employed to more clearly and fully depict the structure and process of the invention than would otherwise be possible.

DEPR:
In parallel with the solvent and concentration control step 83, the substrate 18 is prepared. If the substrate is a metallized substrate, such as the substrate 18, then the substrate is provided in step 85A by forming the layers 22, 24, 26, and 28 and is then prebaked in step 86A. If the substrate is a non-metallized substrate, such as a silicon or gallium arsenide single crystal, the substrate is provided in step 85B and dehydrated in step 86B. In step 87 the substrate is coated with the precursor. In the examples discussed below, the coating was done by a spin-on process, though a process such as a misted deposition process as described in U.S. patent application Ser. No. 993,380, which is hereby incorporated by reference, or dipping or other suitable coating process may be used. The coated substrate is then dried in step 88, and the baked in an RTP (rapid thermal processor) unit. If the desired thickness of the layer 30 is not obtained, then the series of coat, dry, and RTP bake steps

87, 88, and 89 are repeated as many times as required to build up the desired thickness. The wafer 10 is then annealed in step 92, the top or second **electrode** 32 is deposited in step 93 by sputtering or other suitable process, and the wafer 10 is then annealed again in step 94. The capacitor 16 is then structured by ion milling, chemical etching, or other suitable process in step 95. Then follows a third anneal in step 96. This completes the process if a capacitor device as in FIG. 2 is the desired end result, however in the case of an integrated circuit as in FIG. 4, there follows completion steps 97 such as contact metalization, capping, etc. As will be discussed further below, not all of the steps outlined above are necessary for every device: some steps are optional and others are used only for certain layered superlattice materials.

DEPR:
Once the desired film thickness has been obtained, the dried and preferably baked film is annealed in step 92, which is referred to as a first anneal to distinguish it from subsequent anneals. The first anneal is preferably performed in an oxygen atmosphere in a furnace. The oxygen concentration is preferably 20% to 100%, and the temperature is above the crystallization temperature of the particular layered superlattice material 30. Generally, for the materials of the invention, this temperature is above 700.degree. C. To prevent evaporation of elements from the layered superlattice material 30 and to prevent thermal damage to the substrate, including damage to integrated circuits already in place, the annealing temperature is preferably kept below 850.degree. C. Preferably the annealing for strontium bismuth tantalate is done at about 800.degree. C. for 30 to 90 minutes, and is in a similar range for most other layered superlattice materials. Again, the presence of oxygen

is important in this first anneal step. The numerous nuclei, small grains generated by the RTP bake step, grow, and a well-crystallized **ferroelectric** film is formed under the oxygen-rich atmosphere.

DEPR:
After the first anneal, the second or top **electrode** 32 is formed. Preferably the **electrode** is formed by RF sputtering of a platinum single layer, but it also may be formed by DC sputtering, ion beam sputtering, vacuum deposition or other appropriate deposition process. If desirable for the electronic device design, before the metal deposition, the layered superlattice material 30 may be patterned using conventional photolithography and etching, and the top **electrode** 32 is then patterned in a second process after deposition. In the examples described herein, the top **electrode** 32 and layered superlattice material 30 are patterned together using conventional photolithography techniques and ion beam milling.

DEPR:
As deposited, the adhesion of the top **electrode** 32 to the layered superlattice material is usually weak. Preferably, the adhesion is improved by a heat treatment. The wafer 10 including the layered superlattice film 30 covered by the top **electrode** 32 may be annealed before the patterning step 95 described above in a heat treatment designated in FIG. 1 as the second anneal (1) step 94, after the patterning step 95 by a heat treatment designated in FIG. 1 as the second anneal (2) step 96, or both before and after the patterning step 95. The second anneal is preferably performed in an electric furnace at a temperature between 500.degree. C. and the first anneal temperature. A second anneal below 500.degree. C. does not improve the adhesion of **electrode** 32, and the resulting capacitor devices are sometimes extremely leaky, and shorted in

the worst cases.

DEPR:
The second anneal releases the internal stress in the top **electrode** 32 and in the interface between the **electrode** 32 and the layered superlattice material 30. At the same time, the second annealing step 94, 96 reconstructs microstructure in the layered superlattice material 30 resulting from the sputtering of the top **electrode**, and as a result improves the properties of the material. The effect is the same whether the second anneal is performed before or after the patterning step 95. The effect of oxygen ambient during the second anneal is not as clear as it is in the case of RTP bake 89 and the first anneal 92, because the layered superlattice material 30 is covered by the top **electrode** and not exposed to the ambient atmosphere. With regard to most electrical properties, inert gas, such as helium, argon, and nitrogen may be used with approximately the same result as with oxygen. However, it has been found that an oxygen atmosphere during the second anneal improves the crystallographic order at the interface of the **electrode** 32 and layered superlattice material 30 as well as the symmetry of the hysteresis curve.

DEPR:
Below, examples of the fabrication process according to the invention as applied to a wafer 10 as shown in FIGS. 2 and 3 are given. Following each of the examples, there is a discussion of the electrical/electronic properties illustrated in the figures. The figures include hysteresis curves, such as FIG. 5, and material endurance or "fatigue" curves such as FIG. 6. The hysteresis curves are given in terms of either the applied voltage in volts, as for example in FIG. 5, or the electric field in kilovolts per centimeter, as for example in FIG. 7, versus the polarization charge in

microcoulombs per centimeter squared. Generally, the hysteresis is shown for three different voltages (or fields) generally, 2 volts, 4 volts, and 6 volts. As is well-known, hysteresis curves which suggest good **ferroelectric** properties tend to be relatively boxy and long in the direction of polarization, rather than thin and linear. The hysteresis measurements were all made on an uncompensated Sawyer-Tower circuit unless otherwise noted. The endurance or "fatigue" curves give the polarization charge, 2Pr, in microcoulombs per square centimeter versus the number of cycles. The polarization charge 2Pr is the charge created by switching a capacitor such as 16 from a state where it is fully polarized in one direction, say the upward vertical direction in FIG. 3, to the opposite fully polarized state, which would be the downward vertical direction in FIG. 3. Here, by "fully polarized" means the state in which the **ferroelectric** material has been polarized fully and the field removed. In terms of an hysteresis curve, such as shown in FIG. 5, it is the difference between Pr.sub.+, the point where the hysteresis curve crosses the positive polarization axis (y-axis), and Pr.sub.-, the point where the hysteresis curve crosses the negative polarization axis. Unless otherwise noted, the value of 2Pr given is taken from the hysteresis measurement at the highest voltage. The higher the value of 2Pr, the better will be the performance of the material in **ferroelectric** memories and other applications. A cycle is defined as the capacitor, such as 16, being switched through one square pulse. This polarization, 2Pr, is approximately twice the remnant polarization, Pr. Other figures, such as FIG. 11, also show the value 2Ec, which is given in kilovolts per cm, versus some other parameter, such as the amount of bismuth in the stoichiometry (FIG. 11). The parameter 2Ec is equal to the sum

of the coercive field on the positive side, Ec+, and the coercive field on the negative side, Ec-, upon a voltage change, generally taken as from -6 to +6 volts for the figures shown. The coercive field is a measure of the size of the field that is required to switch the material from one polarization state to another. For a practical electronic device, it should be high enough that stray fields will not cause polarization switching, but if it is too high, large voltages will be required to operate the device. Other parameters and terms used in the figures and discussion should be clear from the context.

DEPR:
Further, from FIG. 9, the value of 2Pr is consistently and significantly higher for the 10% excess bismuth samples than for the stoichiometric samples. FIG. 34 shows a graph of 2Pr versus anneal time for samples of strontium bismuth tantalate using a stoichiometric precursor as compared to samples using a 20% excess bismuth precursor. The 20% excess bismuth content material reaches a higher ultimate 2PR value than either the stoichiometric sample or the 10% excess bismuth sample of FIG. 9, although the maximum is reached after a longer annealing time. However, for any given annealing time, the 2Pr of the 20% excess bismuth sample stays well above that for the stoichiometric sample. This superior performance in the samples with excess bismuth in the precursor solution is believed to be due to the fact that bismuth and bismuth oxide have a higher vapor pressure (lower vapor point) than the other metals in the layered superlattice material and the oxides of these other metals. Since the thin film preparation process includes several heating steps, some at relatively high temperatures, the bismuth and bismuth oxide are easily vaporized during the fabrication process. As a result, some bismuth is lost during the process, and if a stoichiometric proportion of bismuth

was present
in the mixed precursor, there will be less than a stoichiometric amount in the
completed thin film, and the resulting layered superlattice material will have
many defects, especially on the surface, with resulting degradation of the
crystalline state and the **ferroelectric** properties that depend on that state.
The excess bismuth compensates for the loss of bismuth during fabrication,
resulting in a more nearly stoichiometric thin film and improved **ferroelectric**
properties. The effect of excess bismuth content on the properties of
strontium bismuth tantalate was studied more thoroughly in a second variation
of the process of the invention utilizing a bismuth gradient, which will be
discussed below. As will be seen, this variation overcomes the problem of the
long annealing time required to reach the maximum 2Pr for the excess bismuth
samples.

DEPR:
Hysteresis curves for each of the ten samples made according to the process of
Example 2 are shown in FIG. 10. As indicated above, all were prepared with an
RTP bake at about 725.degree. C. The values of 2Pr and 2Ec taken from the 6
volt hysteresis curves are plotted in FIG. 11. The graph shows that the
material is clearly **ferroelectric** above 50% of stoichiometry. As the amount of
bismuth increases, so does 2Pr and 2Ec. At about 100% of stoichiometry, 2Ec
peaks and then decreases steadily until it becomes relatively flat at about
130% of stoichiometry. 2Pr peaks at about 120% of stoichiometry [.alpha.0.4 in
the formula (I) or (I')] and then decreases gradually. The upper limit of
bismuth concentration is defined by the electrical shorting of the thin film
due to the degradation of film quality caused by excessive grain growth or
migration of excess bismuth. FIG. 12 is a graph showing the fatigue of the

samples of Example 2 having the different bismuth concentrations. All of the samples show excellent resistance to fatigue, which property does not depend on the bismuth content as long as the material is **ferroelectric**.

DEPR:
FIG. 13 shows a graph of 2Pr and 2Ec for the samples of Example 3 versus the first anneal temperature. The sample annealed at 800.degree. C. shows improved **ferroelectric** performance even though it was annealed for a much shorter time. Thus annealing temperature is critical. Below 650.degree. C., the crystallization does not proceed even if the film had been previously RTP baked at a high temperature.

DEPR:
FIG. 22 is a graph of the hysteresis curves for six different samples of strontium bismuth tantalum titanate (TiTa) having the following percentages of Ti: 100% (SrBi.sub.4 Ti.sub.4 O.sub.15); 80%; 50%; 33%; 20%; and 0% (SrBi.sub.2 Ta.sub.2 O.sub.9). The voltages at which the hysteresis curves were run was 2, 4, and 6 volts as before. In this instance, while both the strontium bismuth titanate and the strontium bismuth tantalate are excellent ferroelectrics, solid solutions of the two near 50/50 ratios are not. Moreover a broad range of **ferroelectric** properties, such as values of 2Pr and 2Ec are represented near the two extremes of the solid solutions.

DEPR:
FIG. 23 is a graph of the hysteresis curves for six different samples of strontium bismuth niobium titanate (TiNb) having the following percentages of Ti: 100% (SrBi.sub.4 Ti.sub.4 O.sub.15); 80%; 50%; 33%; 20%; and 0% (SrBi.sub.2 Nb.sub.2 O.sub.9). The voltages at which the hysteresis curves were run was 2, 4, and 6 volts as before. Again, while both the strontium bismuth titanate and the strontium bismuth niobate are excellent ferroelectrics, solid

solutions of
the two near 50/50 ratios are not. Also a broad range of
ferroelectric
properties, such as values of 2Pr and 2Ec are represented near
the two extremes
of the solid solutions.

DEPR:
All three of the materials strontium bismuth tantalate (Ta),
strontium bismuth
niobate (Nb), and strontium bismuth titanate (Ti) may be mixed in
solid
solution in arbitrary ratio, making a single mixed **ferroelectric**
phase, which
can be represented by the following general formula:
SrBi.sub.4-2x
[(Ta.sub.y,Nb.sub.1-y).sub.x, Ti.sub.2-2x].sub.2 O.sub.15-6x,
where x and y
can take on any value between 0 and 1. FIG. 24 is a graph of the
hysteresis
curves for six different samples of TiTaNb having the following
percentages of
Ti/Ta/Nb: 100%/0%/0% (SrBi.sub.4 Ti.sub.4 O.sub.15); 81%/10%/09%;
52%/25%/23%;
35%/34%/31%; 14%/45%/41%; and 0%/50%/50% (SrBi.sub.2
TaNbO.sub.9). The
voltages at which the hysteresis curves were run was 2, 4, and 6
volts as
before. Again, while strontium bismuth titanate and strontium
bismuth tantalum
niobate are excellent ferroelectrics, solid solutions of the two
near 50/50
ratios are not. Again, a broad range of **ferroelectric**
properties, such as
values of 2Pr and 2Ec are represented near the two extremes of
the solid
solutions.

DEPR:
FIG. 25 is a three dimensional diagram (represented in
two-dimensions) showing
2Pr of most of the different layered superlattice materials and
solid solutions
fabricated and discussed in the above examples. Many patterns
emerge from this
diagram, including the one discussed in relation to FIG. 18, i.e.
the rise of
2Pr from 100% Ta to 100% Nb, the generally lower value of 2Pr
toward the center
of the diagram, and others that were not evident from the

isolated data, such as the rise in 2Pr along the 50% Ti line as it goes from 50% Ta to 50% Nb. Such patterns permit one to use records such as FIG. 25 to design **ferroelectric** devices having specific, predictable properties.

DEPR:
Zirconium is in the same transition metal column of the periodic table of the elements as titanium and can be easily substituted for titanium in a layered superlattice crystal structure in an arbitrary amount. FIG. 30 is a graph of the hysteresis curves for six different samples of ZrTi having the following percentages of Zr:0% (SrBi.sub.4 Ti.sub.4 O.sub.15); 20%; 40%; 50%; and 60%. The voltages at which the hysteresis curves were run was 2, 4, and 6 volts as before. In this case, the **ferroelectric** properties disappear if more than 50% zirconium is added. This does not mean that the material with more than 50% Zr is not a layered superlattice material; it may merely mean that the **ferroelectric** transition temperature changes so that the material is no longer **ferroelectric** at room temperature, and/or that the material becomes a layered superlattice dielectric material. FIG. 31 is a graph of 2Pr and 2Ec as a function of Zr percentage, while FIG. 32 shows the fatigue curves for the material with 10% Zr and the material with 20% Zr. The figures show that while 2Pr and 2Ec decrease close to linearly with the addition of Zr, the resistance to fatigue improves with the addition of Zr, at least up to 20%. Thus Zr also offers opportunities for device design.

DEPR:
As indicated above, lead, thallium and antimony are also elements that form compounds that vaporize easily. Lead bismuth titanate and lead bismuth tantalate are layered superlattice materials that have been shown to have excellent electronic properties by the present inventors. The

preferable amount of excess lead in the second thin film 30B is from 3 mol % to 20 mol % above stoichiometry. The tolerance for excess bismuth is greater in the layered superlattice materials than the tolerance for lead because the lead/lead oxide is included only in the **ferroelectric** layers of the layered superlattice materials, while in the bismuth/bismuth oxide is included in both the **ferroelectric** layers and the non-**ferroelectric** layers; that is, the bismuth is distributed throughout the material while the lead is distributed only in alternate layers.

CLPR:
1. A **ferroelectric** device including a layered superlattice material compound comprising A-site metal and a plurality of B-site metals selected from the group consisting of titanium, tantalum and niobium, said compound having a polarizability 2P, of at least about 15 microcoulombs per square centimeter, said compound being in a film having a thickness not greater than about 3500 .ANG..

CLPR:
2. A **ferroelectric** device as in claim 1 wherein said layered superlattice material comprises a solid solution of two or more materials from the group comprising strontium bismuth tantalate, strontium bismuth niobate, and strontium bismuth titanate.

CLPR:
4. A layered superlattice material as in claim 3 wherein said material is **ferroelectric**.

CLPR:
5. A **ferroelectric** layered superlattice material compound having a polarizability 2Pr greater than 15 microcoulombs per square centimeter, said **ferroelectric** layered superlattice material compound having a

thickness no
greater than about 3500 .ANG..

CLPR:
6. A **ferroelectric** device as in claim 2 wherein said layered superlattice
material comprises an amount of bismuth, as compared to the amount of other
metals, in excess of the proportion of bismuth in the stoichiometric formula
for said layered superlattice material.

CLPR:
7. A **ferroelectric** device as in claim 6 wherein said amount of bismuth is
between 105% and 140% of the normal stoichiometric amount of bismuth.

CLPR:
8. A **ferroelectric** device as in claim 1 wherein said layered superlattice
material comprises a material having the formula:

CLPR:
9. A **ferroelectric** device as in claim 8 wherein:
0.7.ltoreq.x.ltoreq.1.0,
0.8.ltoreq.y.ltoreq.1.0, and 0.ltoreq..alpha..ltoreq.1.2(2-x).

CLPR:
10. A **ferroelectric** device as in claim 2 wherein said layered superlattice
material has an average grain size of from 200 .ANG. to 2000 .ANG..

ORPL:
Subbarao, "A Family of **Ferroelectric** Bismuth Compounds," J. Phys. Chem. Solids,
Pergamon Press, 1962, vol. 23, pp. 665-676.

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DOCUMENT-IDENTIFIER: US 6165802 A
TITLE: Method of fabricating **ferroelectric** integrated circuit using oxygen to
inhibit and repair hydrogen degradation

APD:
19980417

TTL:
Method of fabricating **ferroelectric** integrated circuit using oxygen to inhibit
and repair hydrogen degradation

ABPL:
An integrated circuit is formed that contains a **ferroelectric** element
comprising metal oxide material containing at least two metals. An
oxygen-recovery anneal is conducted in ambient oxygen at a temperature range
from 300.degree. to 1000.degree. C. for a time period from 20 minutes to 2
hours. The oxygen-recovery anneal reverses the effects of hydrogen degradation
and restores **ferroelectric** properties. The oxygen-recovery anneal is more
effective as the annealing temperature and annealing time increase. Preferably
the metal oxide element comprises a layered superlattice compound. Hydrogen
degradation of the **ferroelectric** properties is minimized when the layered
superlattice compound comprises strontium bismuth tantalum niobate and the
niobium/tantalum mole ratio in the precursor is about 0.4. Hydrogen
degradation is further minimized when at least one of the superlattice
generator-element and the B-site element of the layered superlattice compound
is present in excess of the amounts represented by the balanced stoichiometric
formula of the compound.

BSPR:
The invention relates to a method for fabricating a **ferroelectric** integrated
circuit that reduces or eliminates the degradation of electronic

properties
resulting from hydrogen exposure.

BSPR:
Ferroelectric compounds possess favorable characteristics for use in
nonvolatile integrated circuit memories. See Miller, U.S. Pat. No.
5,046,043. A **ferroelectric** device, such as a capacitor, is useful as a
nonvolatile memory when it possesses desired electronic characteristics, such
as high residual polarization, good coercive field, high fatigue resistance,
and low leakage current. Lead-containing ABO.sub.3 type **ferroelectric** oxides
such as PZT (lead titanate zirconate) and PLZT (lanthanum lead titanate
zirconate) have been studied for practical use in integrated circuits. Layered
superlattice material oxides have also been studied for use in integrated
circuits. See Watanabe, U.S. Pat. No. 5,434,102. Layered superlattice
compounds exhibit characteristics in **ferroelectric** memories that are orders of
magnitude superior to those of PZT and PLZT compounds. While prototypes of
ferroelectric memories have been made successfully with the layered
superlattice compounds, there is as yet no manufacturing process for making
memories using either the ABO.sub.3 type oxides or the layered superlattice
material compounds with the desired electronic characteristics economically and
in commercial quantities. One reason, among others, for the lack of economical
commercial processes for the fabrication of high quality **ferroelectric**
integrated circuits is that the oxide compounds are susceptible to reduction by
hydrogen during hydrogen annealing. Hydrogen annealing is a common step during
CMOS integrated circuit memory fabrication and results in degradation of some
important **ferroelectric** properties.

BSPR:
A typical **ferroelectric** memory device in an integrated circuit

contains a
semiconductor substrate and a metal-oxide **semiconductor**
field-effect transistor
(MOSFET) in electrical contact with a **ferroelectric** device,
usually a
ferroelectric capacitor. A **ferroelectric** capacitor typically
contains a
ferroelectric thin film located between a first or bottom
electrode and a
second or top **electrode,** the electrodes typically containing
platinum. During
manufacture of the circuit, the MOSFET is subjected to conditions
causing
defects in the silicon substrate. For example, the manufacturing
process
usually includes high energy steps, such as ion-mill etching and
plasma
etching. Defects also arise during heat treatment for
crystallization of the
ferroelectric thin film at relatively high temperatures, often in
the range
500.degree.-900.degree. C. As a result, numerous defects are
generated in the
single crystal structure of the **semiconductor** silicon substrate,
leading to
deterioration in the electronic characteristics of the MOSFET.

BSPR:
To restore the silicon properties of the MOSFET/CMOS, the
manufacturing process
typically includes a hydrogen annealing step, in which defects
such as dangling
bonds are eliminated by utilizing the reducing property of
hydrogen. Various
techniques have been developed to effect the hydrogen annealing,
such as
H.sub.2 -gas heat treatment in ambient conditions.
Conventionally, hydrogen
treatments are conducted between 350.degree. and 550.degree.
C., typically
around 400.degree. C. for a time period of about 30 minutes. In
addition,
there are several other integrated circuit fabrication processes
that expose
the integrated circuit to hydrogen, often at elevated
temperatures, such as CVD
processes for depositing metals, growth of silicon dioxide from
silane or TEOS
sources, and etching processes using hydrogen. During processes
that involve

hydrogen, the hydrogen diffuses through the top **electrode** and the side of the capacitor to the **ferroelectric** thin film and reduces the oxides contained in the **ferroelectric** material. The absorbed hydrogen also metallizes the surface of the **ferroelectric** thin film by reducing metal oxides. As a result of these effects, the electronic properties of the capacitor are degraded. This problem is acute in **ferroelectric** memories containing layered superlattice compounds because these oxide compounds are particularly complex and prone to degradation by hydrogen-reduction.

BSPR:
The invention solves the above problem by providing a method for fabricating **ferroelectric** elements in integrated circuits that reduces the detrimental effects of the hydrogen and preserves the favorable electronic properties of the **ferroelectric** element.

BSPR:
One aspect of the invention is performing an oxygen-recovery anneal to reoxidize chemical compounds in the **ferroelectric** element that were reduced during manufacturing steps causing hydrogenating and reducing conditions. The oxygen-recovery anneal is typically performed in the temperature range from 300.degree. C. to 1000.degree. C. for a time period from 20 minutes to 2 hours.

BSPR:
Another aspect of the invention is that the **oxygen**-recovery **anneal** is ambient tolerant, that is, it can be performed at atmospheric pressure with **oxygen** gas mixtures containing common ambient gases, such as **nitrogen**.

BSPR:
Another aspect of the invention is formation of a hydrogen barrier layer directly over at least a portion of the **ferroelectric** element.

BSPR:
In a preferred method, a nitride of titanium or silicon is formed to cover the protected portion of the **ferroelectric** element and serve as a hydrogen barrier.

BSPR:
Another aspect of the invention is formation of a **ferroelectric** thin film comprising a layered superlattice compound.

BSPR:
Another aspect of the invention is forming a **ferroelectric** element having layered superlattice compounds containing the chemical elements bismuth, strontium, niobium and tantalum in which the relative amounts of the chemical elements are selected to minimize the degradation of electronic properties by hydrogen.

BSPR:
Another aspect of the invention is formation of a **ferroelectric** thin film in which the layered superlattice compound comprises strontium bismuth tantalum niobate.

BSPR:
Another aspect of the invention is formation of a **ferroelectric** thin film in which the **ferroelectric** thin film comprising strontium bismuth tantalum niobate contains relative amounts of niobium and tantalum selected to inhibit hydrogen degradation of the **ferroelectric** material.

BSPR:
Another aspect of the invention is formation of a **ferroelectric** thin film in which at least one of said metals is present in an excess amount up to forty percent greater than the amount corresponding to a balanced stoichiometric formula.

BSPR:
Another aspect of the invention is formation of a **ferroelectric** thin film in

which the **ferroelectric** thin film comprising strontium bismuth tantalum niobate contains an excess amount of at least one of the metals from the group comprising bismuth and niobium to inhibit hydrogen degradation of the **ferroelectric** material.

BSPR:
A further aspect of the invention is the formation of a **ferroelectric** capacitor with a top **electrode, a ferroelectric** thin film and a bottom **electrode**.

DRPR:
FIG. 1 is a cross-sectional view of a portion of an integrated circuit as may be fabricated by the method of the invention showing a nonvolatile **ferroelectric** memory cell;

DRPR:
FIG. 2 is a flow chart showing the preferred embodiment of a process for fabricating a nonvolatile **ferroelectric** memory device according to the invention;

DEPR:
It should be understood that the FIGS. 1, 3 and 4 depicting **ferroelectric** integrated circuit devices are not meant to be actual plan or cross-sectional views of any particular portion of an actual integrated circuit device. In the actual devices the layers will not be as regular and the thickness may have different proportions. The various layers in actual devices often are curved and possess overlapping edges. The figures instead show idealized representations which are employed to depict more clearly and fully the structure and process of the invention than would otherwise be possible. Also, the figures represent only one of innumerable variations of **ferroelectric** devices that could be fabricated using the method of the invention. FIG. 1 depicts a **ferroelectric** memory containing a switch in the form of

a field
effect transistor in electrical connection with a **ferroelectric** capacitor.
But, it would also be conceivable to use the method of this invention to
fabricate a **ferroelectric** FET memory in which the **ferroelectric** element is
incorporated in the switch element. Such a **ferroelectric** FET is described in
McMillan, U.S. Pat. No. 5,523,964, which is incorporated herein by reference.
Likewise, other integrated circuits fabricated using the method of the
invention could include other elements and compositions of material.

DEPR:
Directing attention to FIG. 1, there is shown a cross-sectional view of an
exemplary nonvolatile **ferroelectric** memory cell that could be fabricated
according to the method of the invention. The general manufacturing steps for
fabricating integrated circuits containing MOSFETs and **ferroelectric** capacitor
elements is described in Yoshimori, U.S. Pat. No. 5,561,307, which is hereby
incorporated by reference as if completely contained herein. General
fabrication methods have been described in other references also. Therefore,
the elements of the circuit of FIG. 1 will be simply identified here.

DEPR:
In FIG. 1, a field oxide region 104 is formed on a surface of a silicon
substrate 102. A source region 106 and a drain region 108 are formed
separately from each other within silicon substrate 102. A gate insulating
layer 112 is formed on the silicon substrate 102 between the source and drain
regions 106 and 108. Further, a gate **electrode** 110 is formed on the gate
insulating layer 112. These source region 106, drain region 108, gate
insulating layer 112 and gate **electrode** 110 together form a MOSFET 113.

DEPR:
An interlayer dielectric layer (ILD) 114 made of BPSG (boron-doped phosphosilicate glass) is formed on substrate 102 and field oxide region 104. An adhesive layer 116 is formed on a portion of ILD 114, and then a **ferroelectric** thin film capacitor 118 is formed on adhesive layer 116. The adhesive layer 116 is made of, for example, titanium, and typically has a thickness of 200 .ANG..

DEPR:
Ferroelectric capacitor 118 is preferably formed on a conventional wafer 140 that may comprise silicon, gallium arsenide or other **semiconductor**, or an insulator, such as silicon dioxide, glass or magnesium oxide (MgO). The bottom and top electrodes of **ferroelectric** capacitors conventionally contain platinum. It is preferable that the bottom **electrode** contains a non-oxidized precious metal such as platinum, palladium, silver, and gold. In addition to the precious metal, metal such as aluminum, aluminum alloy, aluminum silicon, aluminum nickel, nickel alloy, copper alloy, and aluminum copper may be used for electrodes of a **ferroelectric** memory. Adhesive layers, such as titanium, enhance the adhesion of the electrodes to adjacent underlying or overlying layers of the circuits.

DEPR:
In FIG. 1, the **ferroelectric** capacitor 118 comprises a bottom **electrode** 120 made of platinum and having a thickness of 2000 .ANG. (angstroms), a **ferroelectric** thin film 122 formed on the bottom **electrode** 120, a top **electrode** 124 formed on the **ferroelectric** film 122, made of platinum and having a thickness of 2000 .ANG., and preferably an electrically conductive hydrogen barrier layer 126 formed on the top **electrode** and having a thickness of 500-2000 .ANG.. The hydrogen barrier layer 126 can comprise a

single film, for example, titanium nitride or silicon nitride, or it can contain two or more films, for example, a bottom film of titanium, then a film of titanium nitride followed by a titanium film. If the barrier layer 126 is made from electrically conductive material, such as titanium nitride, and acts as a conducting element, then it is self-aligning. The hydrogen barrier layer can be deposited using a conventional sputtering technique. The composition and structure of the **ferroelectric** thin film 124 is discussed in more detail below.

DEPR:
A second interlayer dielectric layer (ILD) 128 made of NSG (nondoped silicate glass) is formed on ILD 114. A PSG (phospho-silicate glass) film or a BPSG film could also be used in ILD 128. Openings 114a are selectively opened through ILD 114 and ILD 128 to expose the source region 106 and gate region 108. Source **electrode** wiring 130 and drain **electrode** wiring 132 are formed to fill openings 114a. Other openings 128a are selectively opened through ILD 128 to expose the electrically conductive hydrogen barrier layer 126 and the bottom **electrode** 120. Top **electrode** wiring 134 and bottom **electrode** wiring 136 are formed to fill these openings 128a. The drain **electrode** wiring 132 is electrically connected to top **electrode** wiring 134. Each of these wirings 130, 132,134 and 136 is made of Al--Si with a thickness of about 3000 .ANG.. If barrier layer 126 is nonconductive, then it is necessary to remove at least a portion of the barrier layer 126 so that the wiring layer 134 can make electrical contact to top **electrode** 124.

DEPR:
The composition of the **ferroelectric** thin film 124 can be selected from a group of suitable **ferroelectric** materials, including but not limited to: an ABO.sub.3

-type perovskite, such as a titanate (e.g., BaTiO.sub.3, SrTiO.sub.3, PbTiO.sub.3 (PT), PbZrTiO.sub.3 (PZT)) or a niobate (e.g., KNbO.sub.3), and, preferably, a layered superlattice compound.

DEPR:
U.S. Pat. No. 5,519,234 issued May 21, 1996, incorporated herein by reference, discloses that layered superlattice compounds, such as strontium bismuth tantalate, have excellent properties in **ferroelectric** applications as compared to the best prior materials and have high dielectric constants and low leakage currents. U.S. Pat. Nos. 5,434,102 issued Jul. 18,1995 and 5,468,684 issued Nov. 21, 1995, incorporated herein by reference, describe processes for integrating these materials into practical integrated circuits.

DEPR:
The word "substrate" can mean the underlying wafer 102 on which the integrated circuit is formed, as well as any object on which a thin film layer is deposited, such as BPSG layer 114. In this disclosure "substrate" shall mean the object to which the layer of interest is applied; for example, when we are talking about a bottom **electrode**, such as 120, the substrate includes the layers 116 and 114 on which the **electrode** 120 is formed.

DEPR:
The term "thin film" is used herein as it is used in the integrated circuit art. Generally it means a film of less than a micron in thickness. The thin films disclosed herein are in all instances less than 0.5 microns in thickness. Preferably the **ferroelectric** thin films 122 are 1000 .ANG. to 3000 .ANG. thick, and most preferably 1200 .ANG. to 2500 .ANG. thick. These thin films of the integrated circuit art should not be confused with the layered capacitors of the macroscopic capacitor art which are formed by a wholly

different process which is incompatible with the integrated circuit art.

DEPR:
The term "stoichiometric" herein, may be applied to both a solid film of a material, such as a layered superlattice material, or to the precursor for forming a material. When it is applied to a solid thin film, it refers to a formula which shows the actual relative amounts of each element in a final solid thin film. When applied to a precursor, it indicates the molar proportion of metals in the precursor. A "balanced" stoichiometric formula is one in which there is just enough of each element to form a complete crystal structure of the material with all sites of the crystal lattice occupied, though in actual practice there always will be some defects in the crystal at room temperature. For example, both SrBi.sub.2 TaNbO.sub.9 and SrBi.sub.2 Ta.sub.1.44 Nb.sub.0.56 O.sub.9 are balanced stochiometric formulas. In contrast, a precursor for strontium bismuth tantalum niobate in which the molar proportions of strontium, bismuth, tantalum, and niobium are 1, 2.18, 1.44, and 0.56, respectively, is represented herein by the unbalanced "stochiometric" formula SrBi.sub.2.18 Ta.sub.1.44 Nb.sub.0.56 O.sub.9, since it contains excess bismuth beyond what is needed to form a complete crystalline material. In this disclosure an "excess" amount of a metallic element means an amount greater than required to bond with the other metals present to make the desired material, with all atomic sites occupied and no amount of any metal left over. However, as known in the art, because bismuth oxide is highly volatile and significant heat is used in fabricating electronic devices according to the invention, the molar proportion of bismuth in a solid **ferroelectric** layer 122, 422, made according to the process of the invention will generally be less than

that in the stochiometric formula for the precursor. However, the molar proportions of strontium, tantalum, and niobium in **ferroelectric** layer 122, 422, made according to the process of the invention will be very close or identical to the molar proportions given in the stochiometric formula for the precursor. See U.S. Pat. No. 5,434,102 issued to Watanabe et al.

DEPR:
The diagram of FIG. 2 is a flow sheet of the fabrication steps used in this invention to make a **ferroelectric** memory. In step 212, a **semiconductor** substrate is provided on which a switch is formed in step 214. The switch is typically a MOSFET. In step 216, an insulating layer is formed to separate the switching element from the **ferroelectric** element to be formed. In step 218, a bottom **electrode** is formed. Preferably the **electrode** is made of platinum and is sputter-deposited to form a layer with a thickness of about 2000 .ANG.. In the preferred method, an adhesion layer made of titanium or titanium nitride of about 200 .ANG. would be formed in this step prior to depositing the **electrode**. The **ferroelectric** thin film is applied to the bottom **electrode** in step 222. In the preferred method, the **ferroelectric** thin film contains layered superlattice compounds. The **ferroelectric** thin films are preferably applied using a liquid deposition technique, such as spin-coating or a misted deposition method as described in U.S. Pat. No. 5,546,945. In the most preferred method, a spin-on technique is used to form the thin film. In step 220, chemical precursors of the layered superlattice compounds that will form the desired **ferroelectric** thin film are prepared. Usually, a final precursor solution is prepared from commercially available solutions containing the chemical precursor compounds. The preferred method utilizes a precursor

solution containing relative molar proportions of the elements strontium, bismuth, tantalum and niobium corresponding approximately to the formula SrBi.sub.2.18 Ta.sub.1.44 Nb.sub.0.56 O.sub.9, in which the mole ration of niobium to tantalum, Nb/Ta, is about 0.4. Preferably, the concentrations of the various precursors supplied in the commercial solutions are adjusted in step 220 to accommodate particular manufacturing or operating conditions. For example, the stoichiometric amounts of the various elements in a commercial solution for a layered superlattice thin film might be SrBi.sub.2.18 Ta.sub.1.44 Nb.sub.0.56 O.sub.9. It is often desirable, however, to add extra niobium or bismuth to this solution to generate extra oxides that will protect the **ferroelectric** compounds from hydrogen-annealing degradation. The application step 222 is preferably followed by a treatment step 224 which preferably includes a drying step, a crystallization substep at elevated temperatures such as a rapid thermal process, and may include treatment with ultraviolet radiation during or after the application step 222. For example, in a typical spin-on procedure, a coat of the precursor might be applied and dried. Then another precursor coat might be applied and dried. The application and treatment steps 222 and 224 can be repeated several times. The treated film is then annealed in oxygen to form the resulting **ferroelectric** thin film in step 226. Following steps 222-226, the top **electrode** is formed in step 228. Step 228 and other steps would include substeps, such as ion milling and ashing. In the preferred method, a hydrogen barrier layer is formed in step 230 to cover at least the top **electrode** of the capacitor. Typically, the hydrogen barrier layer is titanium nitride, which inhibits diffusion of hydrogen into the **ferroelectric** and which is also electrically conductive.

Since, in most cases, the layers below the **ferroelectric** layer are sufficiently thick to prevent hydrogen diffusion to the **ferroelectric,** the most important hydrogen barrier is a barrier that is deposited in one of the layers directly over the **ferroelectric** thin film. By "directly over" means that the barrier layer is above the **ferroelectric** layer in the vertical direction in FIGS. 1 and 4, and extends the length of the **ferroelectric** layer in the horizontal directions in FIGS. 1 and 4. The term does not mean that the barrier layer is in direct contact with the **ferroelectric** layer. The barrier layer may or may not contact the **ferroelectric** layer. As long as it is directly above a portion of the **ferroelectric** layer, it will protect that portion from hydrogen diffusion. It is also desirable to add a small amount of oxygen to the barrier layer by including a small amount of O.sub.2 -gas in the sputter atmosphere during sputter-deposition of the barrier layer. The resulting oxides that form in the barrier layer protect the **ferroelectric** compounds in the memory device by reacting with the hydrogen that can be present in various manufacturing process steps. In step 232, hydrogen annealing of the workpiece is conducted at a temperature and annealing time chosen to satisfactorily eliminate the defects caused in the silicon substrate by oxidation and to minimize hydrogen degradation of the **ferroelectric** compounds. The hydrogen annealing step is preferably performed with H.sub.2 -gas in ambient conditions because this is less complex than other alternatives, such as hydrogen-plasma annealing. In step 234, the oxygen-recovery anneal of the invention is performed to restore the electronic properties of the **ferroelectric** element that were degraded as a result of hydrogen annealing and other process steps causing hydrogenating or reducing conditions. The circuit would be completed in step 236, which could

include a number of substeps, for example, deposition of an ILD, patterning and
milling, and deposition of wiring layers.

DEPR:
Oxygen-gas recovery annealing performed at a temperature range of from
300.degree. to 1000.degree. C. for a time period from 20 minutes to 2 hours
effectively reverses the degradation of electronic properties caused by
hydrogen reduction in the **ferroelectric** element by reoxidizing the chemical
compounds in the **ferroelectric** element. Nevertheless, it might not always be
possible to accomplish the purpose of the oxygen-recovery anneal, that is, the
repair of hydrogen damage in the **ferroelectric** element and other elements, by
using the inventive oxygen-recovery anneal step. For these reasons, the method
of the invention contemplates the use of various steps to protect the memory
device from damage from hydrogen. These steps can be used in conjunction with
the oxygen-recovery anneal step.

DEPR:
The oxygen-recovery anneal of the present invention is effective in protecting
the electronic characteristics of nonvolatile **ferroelectric** capacitors in which
the **ferroelectric** thin film contains Bi-layered superlattice material made from
a precursor with a composition corresponding approximately to the general
formula SrBi.sub.2.18 Ta.sub.2-x Nb.sub.x, where
0.ltoreq..times..ltoreq.2.
Experiments have shown that the oxygen-recovery anneal treatment is effective
in restoring desired **ferroelectric** properties in layered superlattice compounds
made from a precursor solution with a composition corresponding approximately
to the general stoichiometric formula SrBi.sub.2.18 Ta.sub.1.44 Nb.sub.0.56
O.sub.9, in which the mole ratio Nb/Ta in the precursor is about 0.4.
Experiments have further shown that addition of bismuth or niobium to the

precursor in excess of the relative amounts corresponding to the formula
SrBi.sub.2.18 Ta.sub.1.44 Nb.sub.0.56 O.sub.9 is effective in protecting
desired electronic characteristics from hydrogen degradation. The preferred
method of the invention provides a **ferroelectric** capacitor in which at least
the top **electrode** is covered by a hydrogen barrier layer, preferably containing
titanium nitride.

DEPR:
FIG. 3 is a top view of an exemplary wafer on which thin film capacitors 396,
398 and 400 fabricated on substrate 300 in accordance with the invention are
shown greatly enlarged. FIG. 4 is a portion of a cross-section of FIG. 3 taken
through the lines 4--4, illustrating a thin film capacitor device fabricated in
accordance with the invention. A silicon dioxide layer 404 is formed on a
silicon crystal substrate 402. A titanium adhesion layer 416 is formed on the
silicon dioxide layer 404. Then bottom **electrode** 420 made of platinum is
sputter-deposited on adhesion layer 416. Layer 422 is a **ferroelectric** thin
film, and layer 424 represents the top **electrode** made of platinum.

DEPR:
The capacitors were fabricated from a strontium bismuth tantalum niobate
precursor solution commercially available from Hughes Aircraft Company, Product
No. HAC10475-47. The solution contained amounts of chemical precursors
corresponding to the stoichiometric formula SrBi.sub.2.18 Ta.sub.144
Nb.sub.0.56 O.sub.9. The mole ratio of niobium to tantalum, Nb/Ta, in the
precursor was, therefore, about 0.4. The 0.2 mol/l precursor solution in this
example contained: tantalum 2-ethylhexanoate, bismuth 2-ethylhexanoate,
strontium 2-ethylhexanoate, niobium 2-ethylhexanoate, 2-ethylhexanoate, and
xylene. **Ferroelectric** capacitors containing the layered

superlattice compound
were formed from the precursor solution in general accordance with the method
described in Watanabe, U.S. Pat. No. 5,434,102, which is hereby incorporated
by reference as if wholly contained herein.

DEPR:
A series of p-type 100 Si wafer substrates 402 were oxidized to form a layer of
silicon dioxide 404. A titanium adhesive layer 416 of 200 .ANG. thickness was
sputtered on the substrate, then a bottom platinum **electrode** 420 of 3000 .ANG.
thickness was sputter-deposited on adhesive layer 416. These were annealed 30
minutes in O.sub.2 at 650.degree. C., and dehydrated 30 minutes at 180.degree.
C. in low vacuum. A spincoat of 0.2 molar solution of the strontium bismuth
tantalum niobate compound was deposited on the bottom **electrode** 420 at 1500 rpm
for 30 seconds. This was dehydrated for 1 minute at 160.degree. C.,
increasing to 260.degree. C. for 4 minutes. The sequence of the spincoat and
dehydration steps was repeated. The **ferroelectric** coating was crystallized
using rapid-thermal-annealing (RTA 725.degree. C.30 sec, 100.degree. C./sec).
These steps formed a **ferroelectric** thin film 422 having a thickness of
2100.+-.150 .ANG.. The wafer and deposited layers were given a first anneal
for 60 minutes at 800.degree. C. Platinum was sputter-deposited to make a top
electrode layer 424 with 2000 .ANG. thickness, followed by PR treatment. The
platinum and strontium bismuth tantalum niobate layers were milled to form the
capacitors, and then ashing was performed, followed by a second O.sub.2 anneal
for 30 minutes at 800.degree. C.

DEPR:
The effect of covering the top **electrode** of strontium bismuth tantalum niobate
capacitors with a hydrogen barrier made of titanium nitride was studied. After
hydrogen annealing at 400.degree. C. for 10 and 60 minutes, an

oxygen-recovery
anneal was performed at 400.degree. C. for one hour.

DEPR:
Strontium bismuth tantalum niobate capacitors were again prepared according to
the procedure used in Example 1 from precursor solution obtained from Hughes
Aircraft Company, HAC10709-30. The solution contained amounts of chemical
precursors corresponding to the stoichiometric formula
SrB.sub.2.18 Ta.sub.1.44
Nb.sub.0.56 O.sub.9. The mole ratio of niobium to tantalum, Nb/Ta, in the
precursor was, therefore, about 0.4. The capacitors had an area of 7845
.mu.m.sup.2. Then, thin films of titanium nitride were sputter-deposited about
1800 .ANG. thick on the strontium bismuth tantalum niobate capacitors at
various deposition conditions. The titanium nitride films were deposited on
the top **electrode** of the capacitors using a titanium sputter target with
nitrogen sputter gas at gas pressure of 13 mTorr and at 160, 215, 280 and 350 W
power, base pressure 5.times.10.sup.-7 Torr, during 1 hour sputter time. The
titanium nitride films most effective in protecting the strontium bismuth
tantalum niobate capacitors against hydrogen degradation were the films with
highest density, that is, the films produced at 280 W. These films had a
density of 4.89 grams per cubic centimeter (g/cm) and an electrical resistivity
of about 0.76 milliohms centimeter (m.phi.cm). Auger electron spectroscopy
indicated that there as more than 15 percent (15%) oxygen in the deposited film
of titanium nitride. The sides of the capacitors were not coated with barrier
layers.

DEPR:
The effects of H.sub.2 -annealing are shown in FIGS. 11-13. The samples were
annealed in H.sub.2 (5%)-N.sub.2 ambient at 200.degree. C. for 10, 30 and 60
minutes. FIG. 11 is a graph of normalized remnant polarization,

2Pr/[2Pr(pre-anneal)], measured at 3 volts, plotted as a function of hydrogen annealing time at 200.degree. C. In samples with Nb.gtoreq.0.56 annealed 10 minutes, the 2Pr-value degraded about 45 percent. The degradation was greater in samples with Nb=0, and in all samples annealed longer than 10 minutes. For example, the degradation of remnant polarization was about 60% in the sample with Nb=0, annealed 10 minutes. Degradation was almost complete in all samples annealed for 30 or 60 minutes. FIG. 12 is a graph of normalized coercive field, E.sub.c /E.sub.c (pre-anneal), at 3 volts plotted as a function of hydrogen annealing time at 200.degree. C. It shows that the presence of niobium in the **ferroelectric** precursor inhibits degradation of the E.sub.c -value. FIG. 13 is a graph of leakage current measured at 1 volt plotted as a function of hydrogen annealing time in capacitors made from precursors with different Nb/Ta ratios, indicated by the stoichiometric formula subscript of niobium. The leakage current for Nb=0 and Nb=0.56 is about 10.sup.-7 A/cm.sup.2, which is satisfactory for many circuit applications. The leakage current in capacitors where Nb.gtoreq.1.0 is too high for many, but not all, applications.

DEPR:
The results of other experiments show that additional Bi or Nb protects the strontium bismuth tantalum niobate capacitor against degradation by hydrogen annealing. It is believed that amounts up to forty percent in excess of the amount corresponding to a balanced stoichiometric formula. These extra amounts form additional oxides, and they inhibit hydrogen degradation probably by consuming hydrogen that would otherwise reduce the strontium bismuth tantalum niobate oxides. The high leakage in capacitors annealed at longer times seems to be caused by the additional oxide that is consumed by

hydrogen. Upon its reduction by hydrogen annealing, the additional oxide forms elemental metals in the **ferroelectric** capacitor. The conductive metals then act as a leakage path. This suggests that the preferred fabrication process will use sufficient excess metal to "getter" significant hydrogen in its metal-oxide form, but not enough to provide a leakage path when it is reduced by hydrogen. A result of the inventive oxygen-recovery anneal is reoxidation of the metal to form an insulator.

DEPR:
As discussed above, a primary feature of the invention is to reverse the detrimental effects of hydrogen degradation and recover desirable electronic properties of the **ferroelectric** material by performing an oxygen-recovery anneal after hydrogen process steps. For some integrated circuit devices, an oxygen-recovery anneal will be sufficient to obtain good results. However, in other cases, to obtain **ferroelectric** devices with good electronic properties, it is necessary to utilize additional measures. For example, hydrogen degradation can be inhibited by limiting the exposure to hydrogen, which includes exposures at temperatures under 350.degree. C. and for times less than 30 minutes. The use of a hydrogen barrier during hydrogen treatments is also effective in protecting desired electronic properties against hydrogen degradation. As shown in Example 3 above, hydrogen degradation can be minimized by selectively choosing the relative amounts of components comprising the **ferroelectric** device. Similarly, good **ferroelectric** properties can be obtained by using precursors with selectively chosen amounts of excess metal oxide, such as excess bismuth oxide and/or excess niobium oxide.

DEPR:
Further, use of additional oxygen in integrated circuit layers

laid down
subsequent to the **ferroelectric** layers, such as an insulating layer laid down
subsequent to the fabrication of the **ferroelectric** layer, which oxygen acts as
a getter for hydrogen during subsequent hydrogen treatments, can also be
effectively used either alone or in combination with one or more of the above
measures. In this manner, the invention provides processes and/or structures
that enable the prevention of the degradation of **ferroelectric** elements in
combination with almost any exposure to hydrogen that is necessary to create
and perfect the other portions of the integrated circuit.

DEPR:
There has been described a method and structure for fabricating **ferroelectric**
integrated circuits that permit exposure to hydrogen and still result in
ferroelectric devices with good electrical properties. It should be understood
that the particular embodiments shown in the drawings and described within this
specification are for purposes of example and should not be construed to limit
the invention which will be described in the claims below. Further, it is
evident that those skilled in the art may now make numerous uses and
modifications of the specific embodiments described, without departing from the
inventive concepts. For example, now that an oxygen-recovery anneal of the
integrated circuit has been identified as an important part of the process for
fabricating **ferroelectric** memory devices, this method can be combined with
other processes to provide variations on the method described. It is also
evident that the steps recited may in some instances be performed in a
different order. Or equivalent structures and process may be substituted for
the various structures and processes described. Consequently, the invention is
to be construed as embracing each and every novel feature and novel combination

of features present in and/or possessed by the fabrication processes,
electronic devices, and electronic device manufacturing methods described.

ORPL:
Article: H. Achard and H. Mace; "Integration of **Ferroelectric** Thin Films For
Memory Applications"; Science and Technology of Electroceramic Thin Films;
Kluwer Academic Publishers, 1995; pp. 353-372, inclusive.

ORPL:
Symposium Abstract: Ilsub Chung, et al.; "Integration of **Ferroelectric**
Capacitors Using Multilayered **Electrode**"; The Tenth International Symposium on
the Applications of Ferroelectrics, Aug. 18-21, 1996, Hilton Hotel, East
Brunswick, NJ, Rutgers University; p. 55.

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Document Listing

Document	Image pages	Text pages	Error pages
US 5206788 A	0	17	0
Total	0	17	0

anneal: $O_2 + Ar$

or $O_2 + N_2$

DOCUMENT-IDENTIFIER: US 5206788 A
TITLE: Series **ferroelectric** capacitor structure for monolithic integrated
circuits and method

APD:
19911212

TTL:
Series **ferroelectric** capacitor structure for monolithic integrated circuits and
method

ABPL:
A **ferroelectric** capacitor for a memory device including a substrate, a bottom
electrode and a top **electrode**. Between the bottom and top electrodes is either
an alternating plurality of layers of **ferroelectric** material and intermediate
electrodes or a plurality of layers of **ferroelectric** material. A method for
forming the same through establishing one layer over the other is also
disclosed.

BSPR:
The present invention is directed to a **ferroelectric** capacitor and method for
forming the same.

BSPR:
The current method for producing **ferroelectric** capacitors for integrated
ferroelectric memories involves depositing a single layer of a ferroelectric/dielectric material between a bottom **electrode** and a top
electrode. See U.S. Pat. Nos. 4,918,654 ("SRAM With Programmable
Capacitance Divider") and U.S. Pat. No. 5,005,102 ("Multilayer Electrodes For
Integrated Circuit Capacitors") assigned to Ramtron Corporation, the assignee
of the present invention. The result is a capacitor having a bottom **electrode,**
a single layer of **ferroelectric** material, and a top **electrode**. A problem with
this configuration is that if a defect is somehow introduced to

either the bottom **electrode or the ferroelectric** layer, such as during the deposition process or during subsequent processing, the defect may propagate through the entire structure. A defect propagates as either the bottom **electrode or ferroelectric** layer is deposited or as the **ferroelectric** layer is annealed and undergoes a phase transformation.

BSPR:
The object of the present invention is to provide a **ferroelectric** capacitor which decreases the probability of a random defect impacting the quality of the **ferroelectric** memory device.

BSPR:
The present invention in one of its aspects is directed to a **ferroelectric** capacitor for use in volatile and nonvolatile **ferroelectric** memories. The present invention is intended to prevent a random defect from propagating throughout the entire structure of a memory device. The capacitor of the present invention achieves this by having a series of ferroelectric/dielectric and intermediate **electrode** layers established sequentially on a bottom **electrode**. A top layer is then established over the series of **ferroelectric** layers.

BSPR:
In another embodiment, a series of ferroelectric/dielectric layers is established on a bottom **electrode,** and a top **electrode** is established over those layers.

BSPR:
Second, as the number of series combinations increases to form the composite capacitor, the ratio of the dielectric thickness compared to the grain size of the dielectric increases. This provides a means to modify the electrical characteristics of the capacitor since the ratio of the grain

boundary to
electrode interface parasitic effects will change.

BSPR:
The present invention is further directed to a method for fabricating the
ferroelectric capacitor of the present invention. In general, the method
comprises a sequence of deposition steps followed by annealing and defining the
structure to form a **ferroelectric** capacitor having either a series of
ferroelectric/dielectric and intermediate **electrode** layers, or a series of only
ferroelectric/dielectric layers.

BSPR:
Considering the method of the present invention in one of its embodiments, the
top **electrode** of the capacitor is defined first, then the dielectric/ferroelectric layers, and finally the bottom **electrode**.

BSPR:
In still a further embodiment of the invented method, the top **electrode** and the
dielectric/ferroelectric layers are defined simultaneously so that they are
coincident. The bottom **electrode** is then defined in a separate step.

DRPR:
FIG. 1 is a cross-sectional view of a **ferroelectric** capacitor produced by the
prior method;

DRPR:
FIG. 2 is a cross-sectional view of a portion of a **ferroelectric** capacitor
showing a bottom **electrode** over a substrate;

DRPR:
FIG. 3a is a cross-sectional view of a portion of the first embodiment of the
present invention showing **ferroelectric** material over the structure of FIG. 2;

DRPR:
FIG. 3b shows the structure of FIG. 3a with an intermediate **electrode** over the

ferroelectric material;

DRPR:
FIG. 3c shows the structure of FIG. 3b with **ferroelectric** material over the
intermediate **electrode** and another intermediate **electrode** over the
ferroelectric material;

DRPR:
FIG. 3d shows the structure of FIG. 3c with further **ferroelectric** material over
the already established layers of **ferroelectric** material and intermediate
electrodes;

DRPR:
FIG. 3e shows the structure of FIG. 3d with a top **electrode** over the further
ferroelectric material;

DRPR:
FIG. 4a shows a cross-sectional view of a portion of the third embodiment of
the present invention wherein the top and intermediate electrodes and the
ferroelectric material are coincident;

DRPR:
FIG. 5b shows a cross-sectional view of the structure of FIG. 5a with layers of
ferroelectric material over the bottom **electrode**;

DRPR:
FIG. 5c shows structure of FIG. 5b with the addition of a top **electrode**;

DRPR:
FIG. 7 shows a plan view of the structure of the first, second and fifth
embodiments of the present invention after the top **electrode** has been
established and defined but before the dielectric has been established; and

DRPR:
FIG. 8 shows a plan view of the structure of the third, fourth and sixth
embodiments of the present invention after the top **electrode** has been

established and defined but before the dielectric has been established.

DEPR:
FIG. 1 shows a cross-sectional view of the structure produced by the current method for fabricating **ferroelectric** capacitors for integrated **ferroelectric** memories. In this structure, a substrate 10 is provided. Over it is a bottom **electrode** or "plate" 20. A single layer of ferroelectric/dielectric material 3 is deposited between the bottom **electrode** 20 and a top **electrode** 40. As stated previously, a defect in the bottom **electrode** or the ferroelectric/dielectric layer can easily propagate throughout the structure, resulting in degraded electrical properties in the capacitor and severely limiting the electrical capability of any memory device the capacitor is incorporated within.

DEPR:
The **ferroelectric** capacitor of the present invention is intended to decrease the probability of a random defect affecting the quality of the capacitor of a memory device in which the capacitor is incorporated. The present invention is illustrated by six embodiments. The six embodiments, illustrated in the drawings, are described below with reference to a method for fabricating each embodiment.

DEPR:
Generally, in FIG. 2, in accordance with the present invention, a bottom layer or **electrode** 20 is established over a substrate 10. The substrate can be comprised of any basic material, such as silicon and silicon dioxide, germanium, gallium arsenide for example, as long as there is not a material mismatch between substrate 10 and bottom **electrode** 20. Substrate 10 can be fabricated by thermal oxidation or chemical vapor deposition (CVD), for example. The bottom **electrode** can be established, for example,

by deposition
or other commonly used techniques. For example, sputtering deposition or
molecular beam epitaxy (MBE) may be used. Bottom **electrode** 20 preferably
comprises platinum (Pt), palladium (Pd), or an alloy of these two materials,
and it has a thickness in the range from 500 .ANG. (50 nm) to 5,000 .ANG.
(500 nm).

DEPR:
One of the embodiments of the present invention is then established over the
bottom **electrode** structure.

DEPR:
The method for fabricating the first embodiment of the present invention is
shown in FIGS. 3a-3g. In this method, a dielectric, such as a **ferroelectric**
material 30a, is established over bottom **electrode** 20, as shown in FIG. 3a.
Ferroelectric material 30a can be established by a number of different methods.
For example, the material can be deposited by sputtering, evaporation, or
chemical vapor deposition (CVD), or a spin-on method such as sol-gel or
metal-organic decomposition (MOD). The composition of the **ferroelectric**
material is preferably a lead zirconate titanate composition having the
chemical composition of Pb(Ti.sub.x Zr.sub.1-x)O.sub.3, wherein x is in the
range from 0.2 to 1.0. Further, the **ferroelectric** material can be doped with,
for example, niobium (Nb) or lanthanum (La) in the range of 0.5% to 5.0%,
atomic percentage.

DEPR:
After **ferroelectric** material 30a has been established, an intermediate
electrode 35a is established over **ferroelectric** material 30a as shown in FIG.
3b. Intermediate **electrode** 35a is preferably established in a manner similar
to that used for bottom **electrode** 20 and can be comprised of a similar

material. The preferred thickness of layer 35a is in the range of 50 .ANG. (5 nm) to 1000 .ANG. (100 nm).

DEPR:
Thereafter, the process of establishing a layer of **ferroelectric** material and another intermediate **electrode** is repeated until the desired number of layers is obtained. These layers can be established in a manner and with material similar to that used in layers 30a and 35a. FIG. 3c shows an example of this structure with one additional layer of **ferroelectric** material 30b and one additional intermediate **electrode** 35b.

DEPR:
A further layer of **ferroelectric** material 30c is then established over the other **ferroelectric** layers 30a, 30b and the intermediate electrodes 35a, 35b, as shown in FIG. 3d. Layer 30c can be established in a manner similar to that used for layer 30a.

DEPR:
The entire structure is then annealed to form the proper **ferroelectric** phase. Annealing may be performed, for example, by a rapid thermal anneal (RTA) or by furnace annealing. The ambient used for the annealing is, for example oxygen, oxygen-**argon**, or oxygen-**nitrogen** mixtures at a temperature in the range of 500.degree. C. to 900.degree. C. Preferably, a furnace **anneal** in 100% **oxygen** for 30 to 90 minutes is done. The anneal is performed to convert the deposited dielectric into a material with **ferroelectric** characteristics.

DEPR:
A top **electrode** 40 is then established over layer 30c. The top **electrode** can be established, for example, by deposition using the same method and material as used in bottom **electrode** 20. Top **electrode** 40 is then defined. **Electrode** 40 may be defined by conventional **semiconductor** fabrication techniques such as

photolithography and plasma, for example. Preferably, the thickness of top
electrode 40 is in the range from 500 .ANG. (50 nm) to 5,000 .ANG. (500 nm).
The resulting structure is shown in FIG. 3e.

DEPR:
The capacitor stack, comprising **ferroelectric** layers 30a, 30b, 30c and
intermediate electrodes 35a, 35b, is then defined. The capacitor stack may,
for example be defined by plasma etching or other aniostropic etch processes.

DEPR:
Bottom **electrode** 20 is then defined, for example by plasma etching.
Preferably, bottom **electrode** 20 is larger in at least one transverse direction
than the capacitor stack. This relationship exists so that subsequent contact
may be made from other circuits or elements to bottom **electrode** 20. FIG. 3f
shows the resulting structure.

DEPR:
In FIG. 3g, a dielectric material 50 is then established over the structure in
order to passivate the edge of the capacitor stack. Dielectric material 50 can
be, for example, silicon dioxide or silicon nitride. Dielectric material 50
can be established, for example, by deposition such as by CVD. Dielectric
material 50 is used to minimize the leakage current of the capacitor. Contact
windows 60, 70 are then defined through dielectric material 50 to top **electrode**
40 and bottom **electrode** 20, respectively. Contact window 60, 70 can be defined
by conventional photopatterning and etching. FIG. 3g illustrates the completed
structure of the first embodiment of the present invention, it being understood
that contacts are to be added.

DEPR:
The method for fabricating the second embodiment of the present invention
includes all the steps in the method for fabricating the first

embodiment.
However, in the method for fabricating the second embodiment, we anneal after
establishing each layer of **ferroelectric** material, instead of annealing the
structure only after establishing the last layer of **ferroelectric** material
(i.e. 30c in FIG. 3d), as in the first embodiment. Accordingly, the diffusion
of active species, such as oxygen and lead oxide, in the second embodiment can
occur from the top surface of each layer as it is annealed. This provides a
much greater opportunity for diffusion than in the first embodiment wherein any
diffusion must occur through the edges of the **ferroelectric** layers.
Preferrably, each anneal is a furnace anneal at a temperature between
500.degree. C. to 800.degree. C. for 30 to 90 minutes.

DEPR:
The preferred embodiment of the present invention is produced utilizing this
method and comprises a capacitor stack having alternating **ferroelectric** layers
and intermediate electrodes preferably with two to four **ferroelectric** layers.

DEPR:
The method for fabricating the third embodiment of the present invention
involves the same steps as were described above, referring to FIGS. 3a-3d, for
the method for fabricating the first embodiment. For example, after
ferroelectric layer 30c is established, the structure is annealed, and top
electrode 40 is then established in a manner similar to that described above in
the method for the first embodiment. However, unlike in the method for
fabricating the first embodiment, in this method the top **electrode** is not
defined at this point in time. Rather, top **electrode** 40 is defined
later--simultaneously with defining the capacitor stack. As a result, the
capacitor structure and the top **electrode** are congruent (coincident) in plan

view (See FIG. 8). Accordingly, one fewer definition step is necessary than in the method for fabricating the first embodiment. Therefore, the manufacturing cost for fabricating this embodiment is less than the cost for fabricating the first embodiment. Unfortunately, this embodiment has a disadvantage in that there is an increased sensitivity to leakage and breakdown at the edges which can cause a higher leakage current or lower breakdown voltage.

DEPR:
After defining the edges of layers 30a, 35a, 30b, 35b, 30c, and 40, the bottom **electrode** 20 is then defined as described above in the method for fabricating the first embodiment. **Electrode** 20 is larger in plan view in at least one dimension then the stack above it (See FIG. 8). FIG. 4a shows the resulting structure.

DEPR:
The method for fabricating this embodiment includes all the steps of the method for fabricating the third embodiment of the present invention (FIGS. 4a, 4b). However, as described in the method for fabricating the second embodiment, in the fabrication of this embodiment, we anneal not only after we establish the last (uppermost) **ferroelectric** layer but also after we establish each **ferroelectric** layer.

DEPR:
The method for fabricating the fifth embodiment involves FIGS. 5a-5d and employs the same steps as shown in FIG. 3a for fabricating the first embodiment wherein **ferroelectric** material 30a is established over bottom **electrode** 20. The structure is then annealed. The annealing can be done using a silicon diffusion furnace system, for example.

DEPR:
A layer of **ferroelectric** material 30b is then established directly over and

upon the upper surface of **ferroelectric** material 30a, as shown in FIG. 5a.
Layer 30b can be established, for example, using the same material and in the
same manner as **ferroelectric** material 30a. The structure is then annealed, for
example, in a manner similar to that used after the establishment of
ferroelectric material 30a.

DEPR:
Still another layer of **ferroelectric** material 30c can be established directly
over and upon the upper surface of **ferroelectric** material 30b, for example,
with materials and in a manner similar to that used for **ferroelectric** material
30a. FIG. 5b shows the resulting structure. The structure is then annealed,
for example, in a manner similar to that used after the establishment of
ferroelectric material 30a. Layers of **ferroelectric** material can be
continually established and annealed until the required total dielectric
thickness is reached. This method of fabrication is advantageous over the
methods for fabricating the first through fourth embodiment because in this
embodiment there ar fewer **electrode**-dielectric interfaces which entail more
difficult manufacturing issues. Therefore, this method of fabrication has
easier manufacturing and process control than in the fabrication methods for
the first through fourth embodiments.

DEPR:
A top **electrode** 40 is then established and defined, for example, as described
in the method for fabricating the first embodiment. Layers of **ferroelectric**
material 30a, 30b, 30c are then defined, for example, in a manner similar to
that disclosed in the method for fabricating the first embodiment. Bottom
electrode 20 is then defined, as described in the first embodiment. The
structure shown in FIG. 5c results.

DEPR:
The method for fabrication of the sixth embodiment of the present invention involves the same steps as were previously described in FIGS. 5a-5b for fabricating the fifth embodiment. In this method of fabrication, annealing is delayed until all the **ferroelectric** layers have been established. Top **electrode** 40 is then established, for example, in the same manner as in the fabrication of the fifth embodiment, but it is not defined at this time. Rather, top **electrode** 40 is defined when the capacitor stack (i.e. layers 30a, 30b, 30c of **ferroelectric** material) is defined. As a result, the capacitor stack and the top **electrode** are coincident (See FIG. 8). The stack can be defined, for example, in the same manner as used in the method for fabrication of the fifth embodiment. Bottom **electrode** 20 is then defined. The structure shown in FIG. 6a results.

DEPR:
FIG. 7 shows a plan view of the structure of the first, second and fifth embodiments after top **electrode** 40 has been established and defined but prior to the establishment of dielectric 50.

DEPR:
FIG. 8 shows a plan view of the structure of the third, fourth and sixth embodiments after top **electrode** 40 has been established and defined but prior to the establishment of dielectric 50.

CLPR:
1. A **ferroelectric** capacitor comprising:

CLPR:
2. The capacitor of claim 1 wherein said top **electrode, said ferroelectric** material and said intermediate **electrode** have lateral edges which are coincident.

CLPR:

3. The capacitor of claim 1 wherein said **ferroelectric** material comprises a lead zirconate titanate composition defined by the chemical composition Pb(Ti.sub.x Zr.sub.1-x)O.sub.3, wherein x is from 0.2 to 1.0.

CLPR:
4. The capacitor of claim 3 wherein said **ferroelectric** material further comprises a dopant.

CLPR:
6. The capacitor of claim 1 wherein said intermediate **electrode** is selected from the group comprising platinum, palladium and an alloy of platinum and palladium.

CLPR:
7. The capacitor of claim 1 wherein a dielectric material is established over said capacitor and contact windows are defined to said top **electrode** and said bottom **electrode**.

CLPR:
8. A **ferroelectric** capacitor comprising:

CLPR:
9. The capacitor of claim 8 wherein said top **electrode, said ferroelectric** material and said intermediate **electrode** have lateral edges which are coincident.

CLPR:
10. The capacitor of claim 8 wherein said **ferroelectric** material comprises a lead zirconate titanate composition defined by the chemical composition Pb(Ti.sub.x Zr.sub.1-x)O.sub.3, wherein x is from 0.2 to 1.0.

CLPR:
11. The capacitor of claim 10 wherein said **ferroelectric** material further comprises a dopant.

CLPR:
13. The capacitor of claim 8 wherein said intermediate **electrode** is selected

from the group comprising platinum, palladium and an alloy of platinum and
palladium.

CLPR:
14. The capacitor of claim 8 wherein a dielectric material is established over
said capacitor and contact windows are defined to said top **electrode** and said
bottom **electrode**.

CLPR:
15. A **ferroelectric** capacitor comprising:

CLPR:
16. The capacitor of claim 15 wherein said **ferroelectric** material comprises a
lead zirconate titanate composition defined by the chemical composition
Pb(Ti.sub.x Zr.sub.1-x) O.sub.3, wherein x is from 0.2 to 1.0.

CLPR:
17. The capacitor of claim 16 wherein said **ferroelectric** material further
comprises a dopant.

CLPR:
19. The capacitor of claim 15 wherein a dielectric material is established
over said capacitor and contact windows are defined to said top **electrode** and
said bottom **electrode**.

CLPR:
20. A method for forming a **ferroelectric** capacitor comprising the steps of:

CLPR:
21. The method of claim 20 wherein first the top **electrode** is defined, then
the layers of **ferroelectric** material and intermediate **electrode** are defined,
and then the bottom **electrode** is defined so that at least one edge of the
bottom **electrode** is unobstructed.

CLPR:
22. The method claim 20 including the step of annealing after the second layer
of **ferroelectric** material is established.

CLPR:
23. The method of claim 20 including the step of annealing after each layer of **ferroelectric** material and intermediate **electrode** is established.

CLPR:
24. The method of claim 20 wherein the top **electrode, the ferroelectric** material and the intermediate **electrode** are all defined at the same time so that the edges of each are coincident.

CLPR:
25. The method of claim 20 including the step of establishing a dielectric material over said capacitor and defining contact windows through said dielectric material to said top **electrode** and said bottom **electrode**.

CLPR:
26. A method for forming a **ferroelectric** capacitor comprising the steps of:

CLPR:
27. The method of claim 26 wherein first the top **electrode** is defined, then the layers of **ferroelectric** material are defined, and then the bottom **electrode** is defined so that at least one edge of the bottom **electrode** is unobstructed.

CLPR:
28. The method of claim 26 wherein the top **electrode** and layers of **ferroelectric** material are defined at the same time so that the edges of each layer are coincident.

CLPR:
29. The method of claim 26 including the step of annealing after said plurality of layers of **ferroelectric** material have been established.

CLPR:
30. The method of claim 26 including the step of annealing after each layer of **ferroelectric** material is established.

CLPV:
a bottom **electrode** over said substrate;

CLPV:
a first layer of a **ferroelectric** material over said bottom **electrode**;

CLPV:
an intermediate **electrode** over said first layer of **ferroelectric** material;

CLPV:
a second layer, distinct from said first layer, of **ferroelectric** material, said
second layer being located over said intermediate **electrode**; and

CLPV:
a top **electrode** over said second **ferroelectric** material.

CLPV:
a bottom **electrode** over said substrate;

CLPV:
an alternating plurality of distinct layers of **ferroelectric** material and
intermediate electrodes located over said bottom **electrode**;

CLPV:
another layer, distinct from said layers of **ferroelectric** material, of
ferroelectric material, said another layer being located over said alternating
plurality of layers; and

CLPV:
a top **electrode** over said another layer of **ferroelectric** material.

CLPV:
a bottom **electrode** over said substrate;

CLPV:
a plurality of layers of **ferroelectric** material over said bottom **electrode**,
each of said plurality of layers located directly over each other; and

CLPV:
a top **electrode** over said plurality of layers of **ferroelectric**

material.

CLPV:
establishing a bottom **electrode** over said substrate;

CLPV:
establishing a first layer of **ferroelectric** material over said bottom
electrode;

CLPV:
establishing an intermediate **electrode** over said layer of **ferroelectric**
material;

CLPV:
establishing a second layer of **ferroelectric** material, distinct from said first
layer, over said intermediate **electrode**; and

CLPV:
establishing a top **electrode** over said second layer of **ferroelectric** material.

CLPV:
establishing a bottom **electrode** over said substrate;

CLPV:
establishing a plurality of layers of **ferroelectric** material over said bottom
electrode, each of said plurality of layers being located directly over one
another; and

CLPV:
establishing a top **electrode** over said layers of **ferroelectric** material.

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1	BRS	L81	7	(ANNEAL with oxygen with (nitrogen or argon or inert)) AND FERROELECTRIC AND ELECTRODE AND (@AD <= "19991029") and semiconductor	USPAT	2001/01/16 14:27			0
2	BRS	L82	57	((ANNEAL WITH OXYGEN) and (ARGON OR INERT OR NITROGEN)) AND FERROELECTRIC AND (@AD <= "19991029") AND SEMICONDUCTOR AND ELECTRODE	USPAT	2001/01/16 14:26			0
3	BRS	L83	3	((((ANNEAL WITH OXYGEN) WITH (ARGON OR INERT OR NITROGEN)) AND FERROELECTRIC) AND (@AD <= "19991029") AND SEMICONDUCTOR AND ELECTRODE) and 438/240.ccls.	USPAT	2001/01/16 14:25			0
4	BRS	L84	311	((((ANNEAL WITH OXYGEN) AND FERROELECTRIC) AND (@AD <= "19991029")) AND (ARGON OR INERT OR NITROGEN) AND SEMICONDUCTOR AND ELECTRODE) 438/240.ccls.	USPAT	2001/01/16 14:26			0
5	BRS	L85	3	((((ANNEAL WITH OXYGEN) WITH (ARGON OR INERT OR NITROGEN)) AND FERROELECTRIC) AND (@AD <= "19991029") AND SEMICONDUCTOR AND ELECTRODE) and 257/295.ccls.	USPAT	2001/01/16 14:28			0
6	BRS	L86	2	(((257/310.CCLS.) AND ((ANNEAL WITH OXYGEN) WITH (ARGON OR INERT OR NITROGEN)) AND FERROELECTRIC) AND (@AD <= "19991029") AND SEMICONDUCTOR AND ELECTRODE)	USPAT	2001/01/16 14:28			0

	U	1 [1]	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
1	☐	☒	US 6153490 A	20001128	20	Method for forming integrated circuit capacitor and memory	438/396	438/240 ; 438/3 ; 438/669 ; 438/712	
2	☐	☒	US 6140672 A	20001031	21	Ferroelectric field effect transistor having a gate electrode being electrically connected to the bottom electrode of a ferroelectric capacitor	257/295	257/296 ; 257/300 ; 438/3	
3	☐	☒	US 6133092 A	20001017	12	Low temperature process for fabricating layered superlattice materials and making electronic devices including same	438/256	427/100 ; 427/376.2 ; 427/96 ; 438/239 ; 438/3 ; 438/386 ; 438/399	
4	☐	☒	US 6130102 A	20001010	13	Method for forming semiconductor device including a dual inlaid structure	438/3	438/240 ; 438/253	
5	☐	☒	US 5426075 A	19950620	16	Method of manufacturing ferroelectric bismuth layered oxides	438/3	204/192.15 ; 204/192.22 ; 438/785	
6	☐	☒	US 5423285 A	19950613	48	Process for fabricating materials for ferroelectric, high dielectric constant, and integrated circuit applications	117/90	117/88 ; 204/192.35 ; 438/3 ; 438/785	
7	☐	☒	US 5330931 A	19940719	13	Method of making a capacitor for an integrated circuit	438/3	438/396	
8	☐	☒	US 4437139 A	19840313	6	Laser annealed dielectric for dual dielectric capacitor	361/313	204/192.15 ; 204/192.22 ; 29/25.42 ; 427/554 ; 427/79 ; 438/3	

	Inventor	S	C	P	2	3	4	5
1	Xing, Guoqiang , et al.	☒	☐	☐	☐	☐	☐	☐
2	Arita, Koji , et al.	☒	☐	☐	☐	☐	☐	☐
3	Hayashi, Shinichiro , et al.	☒	☐	☐	☐	☐	☐	☐
4	White, Jr., Bruce E. , et al.	☒	☐	☐	☐	☐	☐	☐
5	Perino, Stanley , et al.	☒	☐	☐	☐	☐	☐	☐
6	Paz de Araujo, Carlos A. , et al.	☒	☐	☐	☐	☐	☐	☐
7	Emesh, Ismail T. , et al.	☒	☐	☐	☐	☐	☐	☐
8	Howard, James K.	☒	☐	☐	☐	☐	☐	☐